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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,575	07/17/2003	Jang-Jin Yoo	8733.418.10	8871

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EXAMINER	
RUDE, TIMOTHY L	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 02/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,575	YOO ET AL.	
	Examiner	Art Unit	
	Timothy L Rude	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-20 and 30-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-20 and 30-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/836,352.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20030717*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1-7 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated (typical LCD devices per Specification pages 1-8). See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claims

2. Claims 1-17 and 21-29 are cancelled.

Claim Objections

3. Claim 18 is objected to because of the following informalities: The claim refers to auxiliary pixel electrodes when only a single auxiliary pixel electrode has been claimed. Also, the recitation "pixel electrodes are on a same layer" is unclear as to what else is on the same layer. For examination purposes the auxiliary pixel electrode will be considered singular, and the pixel electrodes will be considered to be on the same layer as the auxiliary pixel electrode. Appropriate correction is required.

Claim 34 is objected to because of the following informalities: The recitation "on the second pass layer" will be considered to be - - on the second passivation layer - -.

Also, the recitation "a plurality of common ... with the pixel electrodes;" is repeated (redundant). Appropriate correction is required.

Claims 31 and 32 are objected to because of the following informalities: They are dependent upon canceled claims. For examination purposes they will be considered to depend from claims 18 and 19 respectively - resulting in a lack basis for "a male electrode". Based upon the specification claims 31 and 32 will be considered to not further limit auxiliary common electrode and auxiliary pixel electrode recitations respectively. Appropriate correction is required.

Claim Rejections - 35 USC § 102

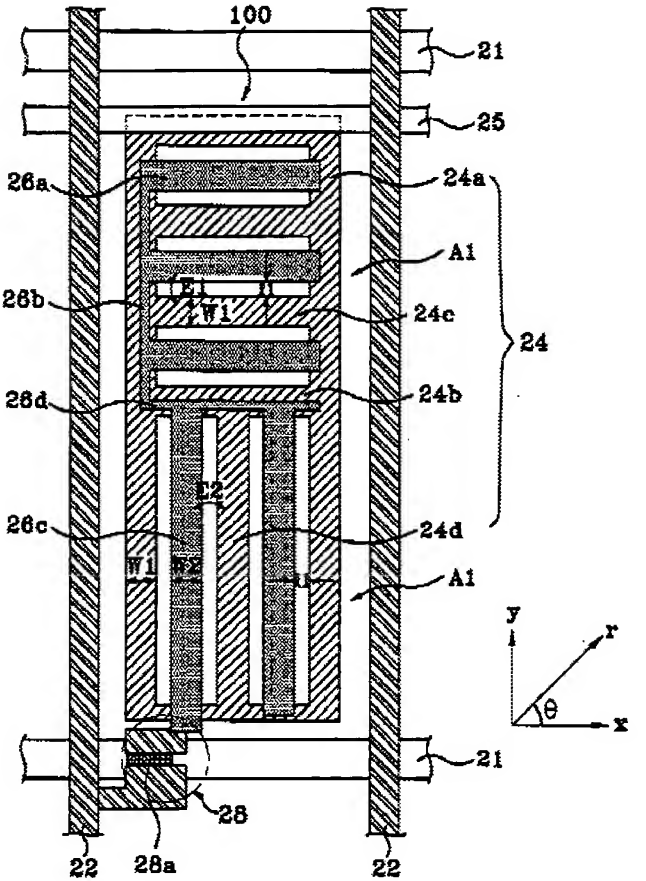
The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 18-20, 31, and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al (Lee) USPAT 6,266,118 B1.

As to claims 18 and 31, Lee discloses (Abstract, Title, entire patent and first embodiment) an array substrate for an IPS-LCD device (col. 6, line 35 through col. 9, line 54), comprising:

FIG.3



a substrate; a gate line, 21, on the substrate; a data line, 22, perpendicular to the gate line; a thin film transistor, 28, at a crossing portion between the gate and data lines; a common line, 25, parallel to the gate line; a plurality of common electrodes, 24d, 24a,

and its counterpart on the left, extending perpendicular to the common line; a plurality of pixel electrodes, 26c and 26b, arranged alternately with the plurality of common electrodes; an auxiliary common electrode, 24c, perpendicularly contacting each of the common electrodes; and an auxiliary pixel electrode, 26d, perpendicularly contacting each of the pixel electrodes; wherein the auxiliary pixel electrode is spaced apart from the auxiliary common electrode; and pixel electrodes are on a same layer as said auxiliary pixel electrode.

As to claims 19 and 32, Lee discloses (Abstract, Title, entire patent and first embodiment) an array substrate for an IPS-LCD device (col. 6, line 35 through col. 9, line 54), comprising: a substrate; a gate line, 21, on the substrate; a data line, 22, perpendicular to the gate line; a thin film transistor, 28, at a crossing portion between the gate and data lines; a common line, 25, parallel to the gate line, the common line including first and second auxiliary common lines, 24d, 24a, and its counterpart on left, perpendicular to the common line; a plurality of common electrodes, 24b and 24c, extending perpendicular to the first and second auxiliary common lines; a plurality of pixel electrodes, 26a and its counterparts, arranged alternately with the plurality of common electrodes; an auxiliary common electrode, 24a (dual purpose), perpendicularly contacting each of the common electrodes; and an auxiliary pixel electrode, 26b, perpendicularly contacting each of the pixel electrodes, wherein the auxiliary pixel electrode is spaced apart from the auxiliary common electrode.

As to claim 20, Lee discloses (Abstract, Title, entire patent and first embodiment) an array substrate for an IPS-LCD device (col. 6, line 35 through col. 9, line 54), comprising: a substrate; a gate line, 21, on the substrate; a data line, 22, perpendicular to the gate line; a thin film transistor, 28, at a crossing portion between the gate and data lines; a common line, 25, parallel to the gate line, the common line including a plurality of common electrodes, 24d, 24a, and its counterpart on the left, extending perpendicular to the common line; a plurality of pixel electrodes, 26c and its counterpart on the right, arranged alternately with the plurality of common electrodes; and a plurality of auxiliary electrodes, 24b, 24c, and 26d, connecting the plurality of common and pixel electrodes in a check pattern.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Hirakata et al (Hirakata) USPAT 5,977,562.

As to claim 33, Lee discloses (Abstract, Title, entire patent and first embodiment) an array substrate for an IPS-LCD device (col. 6, line 35 through col. 9, line 54), above comprising: a substrate; a gate line on the substrate; a gate insulating layer over the gate line; a data line perpendicular to the gate line; a thin film transistor at a crossing portion between the gate and data lines; and a common line parallel to the gate line, the common line including first and second auxiliary common lines perpendicular to the common line; a plurality of common electrodes extending perpendicular to the first and second auxiliary common lines; an auxiliary common electrode perpendicularly contacting each common electrode; and an auxiliary pixel electrode perpendicularly contacting each of the pixel electrodes; wherein the auxiliary pixel electrode is spaced apart from the auxiliary common electrode; and wherein the pixel electrodes are arranged alternately with the common electrodes.

Lee does not explicitly disclose a first passivation layer over the gate insulating layer, the data line and thin film transistor; a plurality of pixel electrodes on the first

passivation layer; a second passivation layer over the pixel electrodes; a common line on the second passivation layer.

Hirakata teaches in the fourth embodiment (col. 8, line 56 through col. 9, line 34) a dielectric film, 205 (Applicant's first passivation layer), over the gate insulating layer, the data line and thin film transistor; a plurality of pixel electrodes, 321, on the first passivation layer; a second dielectric film, 206 (Applicant's second passivation layer), over the pixel electrodes; a common line, 322, on the second passivation layer to comprise a structure with increased aperture ratio (col. 8, lines 57-59).

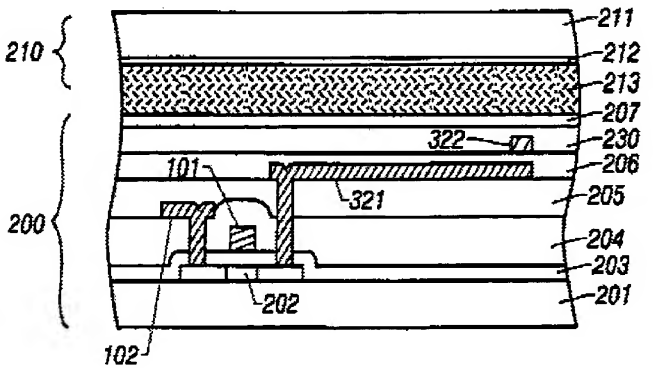


FIG. 10

Hirakata is evidence that ordinary workers in the art of liquid crystals would find the reason, suggestion, or motivation to add a first passivation layer over the gate insulating layer, the data line and thin film transistor; a plurality of pixel electrodes on the first passivation layer; a second passivation layer over the pixel electrodes; a common

line on the second passivation layer to comprise a structure with increased aperture ratio.

Therefore, it would have been obvious to one having ordinary skill in the art of liquid crystals at the time the invention was made to modify the LCD of Lee with the first passivation layer over the gate insulating layer, the data line and thin film transistor; a plurality of pixel electrodes on the first passivation layer; a second passivation layer over the pixel electrodes; a common line on the second passivation layer of Hirakata to comprise a structure with increased aperture ratio.

As to claim 34, Lee discloses (Abstract, Title, entire patent and first embodiment) an array substrate for an IPS-LCD device (col. 6, line 35 through col. 9, line 54), above comprising: a substrate; a gate line on the substrate; a gate insulating layer on the gate line; a data line perpendicular to the gate line; a thin film transistor at a crossing portion between the gate and data lines; common electrodes perpendicular to the common line and arranged alternatively with the pixel electrodes; an auxiliary common electrode perpendicularly contacting each of the common electrodes; and an auxiliary pixel electrode perpendicularly contacting each of the pixel electrodes; wherein the auxiliary pixel electrode is spaced apart from the auxiliary common electrode.

Lee does not explicitly disclose a first passivation layer over the gate insulating layer, the data line and thin film transistor; a plurality of pixel electrodes on the first passivation layer; a second passivation layer over the pixel electrodes; a common line on the second passivation layer.

Hirakata teaches in the fourth embodiment (col. 8, line 56 through col. 9, line 34) a dielectric film, 205 (Applicant's first passivation layer), over the gate insulating layer, the data line and thin film transistor; a plurality of pixel electrodes, 321, on the first passivation layer; a second dielectric film, 206 (Applicant's second passivation layer), over the pixel electrodes; a common line, 322, on the second passivation layer to comprise a structure with increased aperture ratio (col. 8, lines 57-59).

Hirakata is evidence that ordinary workers in the art of liquid crystals would find the reason, suggestion, or motivation to add a first passivation layer over the gate insulating layer, the data line and thin film transistor; a plurality of pixel electrodes on the first passivation layer; a second passivation layer over the pixel electrodes; a common line on the second passivation layer to comprise a structure with increased aperture ratio.

Therefore, it would have been obvious to one having ordinary skill in the art of liquid crystals at the time the invention was made to modify the LCD of Lee with the first passivation layer over the gate insulating layer, the data line and thin film transistor; a plurality of pixel electrodes on the first passivation layer; a second passivation layer over the pixel electrodes; a common line on the second passivation layer of Hirakata to comprise a structure with increased aperture ratio.

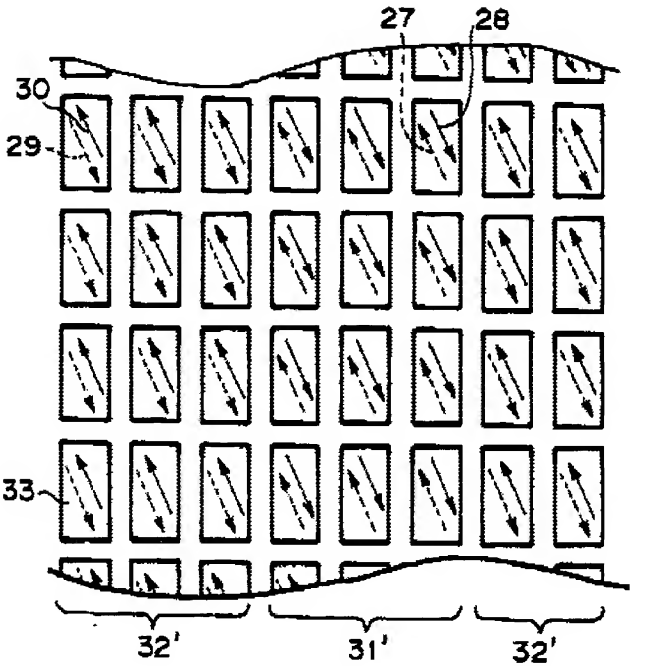
6. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Okamoto et al (Okamoto) USPAT 6,154,266.

As to claim 30, Lee discloses (Abstract, Title, entire patent and first embodiment) an array substrate for an IPS-LCD device (col. 6, line 35 through col. 9, line 54), comprising: a substrate; a gate line, 21, on the substrate; a data line, 22, perpendicular to the gate line; a thin film transistor, 28, at a crossing portion between the gate and data lines; a pixel region surrounded by the gate and data lines, the pixel region including first (upper) and second (lower) domains; transverse pixel and common electrodes disposed on the first domain and parallel to the gate line, the transverse pixel and common electrodes being alternately arranged; perpendicular pixel and common electrodes disposed on the second domain and perpendicular to the transverse pixel and common electrodes, respectively, the perpendicular pixel and common electrodes being alternately arranged.

Lee does not explicitly disclose an alignment layer having first and second rubbing directions, the first and second rubbing directions corresponding to the first and second domains, respectively.

Okamoto teaches (Abstract, Title, entire patent) an alignment layer having first and second rubbing directions, the first and second rubbing directions corresponding to the first and second domains, respectively (col. 3, lines 25-59) to enhance image quality by preventing dependence on the viewing angle in the vertical and right-and-left directions.

FIG. 7



Okamoto is evidence that ordinary workers in the art of liquid crystals would find the reason, suggestion, or motivation to add an alignment layer having first and second rubbing directions, the first and second rubbing directions corresponding to the first and second domains, respectively, to enhance image quality by preventing dependence on the viewing angle in the vertical and right-and-left directions.

Therefore, it would have been obvious to one having ordinary skill in the art of liquid crystals at the time the invention was made to modify the LCD of Lee with the

alignment layer having first and second rubbing directions, the first and second rubbing directions corresponding to the first and second domains, respectively of Okamoto to enhance image quality by preventing dependence on the viewing angle in the vertical and right-and-left directions.

Conclusion

References cited but not applied are relevant to the instant application.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy L Rude whose telephone number is (571) 272-2301. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H Kim can be reached on (703) 305-3492. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

TOANTON
PRIMARY EXAMINER

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Timothy L Rude
Examiner
Art Unit 2871

tlr